March 4 - 6, 2008

CMP-MIC Catalog No.
08 IMIC - 3000P

Fremont Marriott Hotel
Fremont, California

2008 PROCEEDINGS

THIRTEENTH INTERNATIONAL

CHEMICAL-MECHANICAL PLANARIZATION FOR ULSI MULTILEVEL INTERCONNECTION CONFERENCE (CMP-MIC)

A SPECIALTY CONFERENCE OF

2008 MICROELECTRONICS INSTITUTE INTER-ON-CHIP CONNECTION

1µm

Library of Congress No.
89-644090

Bench top dual mode eCMP polisher with multi sensing metrology

V. Khosla, M. Vinogradov
CETR, 1715 Dell Ave, Campbell, CA 95008
info@cetr.com; www.cetr.com

Abstract

A traditional CMP tool is designed to achieve the planarization process across the wafer via a down-force polishing effect. In doing so, the wafer is pressed onto a rotating polishing pad and a slurry material is applied. The traditional CMP process can cause delamination and fracture of low-k dielectrics that are soft and porous. A new alternative a low down-force process of electro-polishing or eCMP is being considered, in which a current is run from a conducting surface, through a conducting liquid and into an electrode. Under proper conditions, metal can be removed from the wafer surface into solution.

As the eCMP is not a mature technology, there are no standard consumables on the market. To develop slurries, pad, particles, conditioners, etc. we have developed a multifunctional bench-top eCMP polisher mod. eCP-4.

The eCP-4 can be used to run both conductive and non-conductive pads. The tool can be used to do polishing in both constant current and constant voltage modes. It has a precise down-force servo-control from 0.05 to 10 psi. The eCP-4 polisher is equipped with multi-sensing metrology which measures in-situ friction force and coefficient in both wafer-pad and conditioner-pad interfaces, contact acoustic emission, applied voltage and current, temperature, pad wear at a 100 kHz data acquisition rate. The same tool can also be used for a regular CMP, which enables to use CMP and eCMP sequentially to completely clear the barrier after copper removal. This paper covers the capabilities of the bench-top eCMP polisher with both conductive and non-conductive pads. We present the data obtained on the eCMP tool and explain the benefits of multi-sensing metrology to develop novel processes and materials for eCMP.

Introduction

The performance of a miniaturized semiconductor device is governed by its signal processing speed, which in turn is determined by the gate and interconnect delay times. For devise features scaled down below 0.5 micron, the interconnect "RC delay" dominates the delay in signal processing, where R is the resistance of the wiring metal and C is the capacitance of the interlayer dielectric (ILD) used in the device. From simple considerations, it can be shown that [1,2] RC = $[(rkl^2)/(yd)]$. Here *r*, *l* and *d* represent the resistivity, length and thickness of the wiring line, respectively; *k* and *y* represent the dielectric function and thickness of the ILD, respectively. Thus, decreasing the value of *l* and/or that of *k* can decrease the delay time. Most of the such low-*k* ILD materials ($k < 2.5$), however, are often porous and mechanically fragile. Therefore, to avoid damages to the ILD during IC fabrication, planarization of the ILD materials and their overlying structures must be performed at a low applied down-pressure (usually at < 1 psi). Although low-P operation is difficult to incorporate in the currently available framework of CMP, it is possible to combine electrochemically controlled material removal with low-P mechanical polishing where the main role of the latter step is to provide uniform planarization across the sample surface.

Thus ECMP can be a technology of choice for future nodes. But as the eCMP is not a mature technology, there are no standard consumables on the market. To develop slurries, pad, particles, conditioners, etc. we have developed a multifunctional bench-top eCMP polisher mod. eCP-4. This bench top polisher uses multi sensing technology to generate data which can enable the researchers to learn and gain more about the process. The tool (shown in figure 1) can be used to polish low k wafers under 0.5 psi range and can accommodate both conductive and non conductive pads. The tool uses multi sensing technology (explained later) and can be used to develop pads, pad conditioner, slurry, process etc.

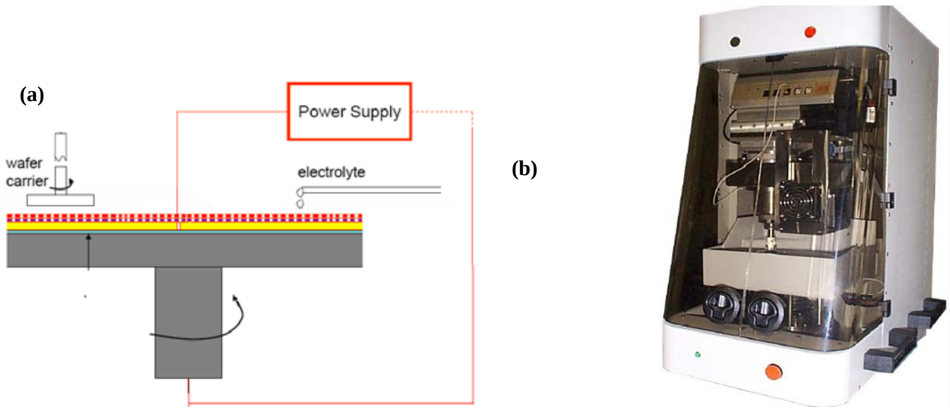

Figure 1 (a) Schematic of eCMP (b) eCP4 tool by CETR

Multi Sensing Technology –. The technology involves measuring insitu Friction, coefficient of friction, downforce acoustic emission, current and voltages and pad wear at all times at 100KHz frequency.

ECMP process can be run at constant voltage or at constant current. The tool is capable to run the process in either mode. Typically the modes are changed as copper thins down to prevent very high voltages at barrier and wafer contact interface. When running in constant voltage mode the tool measure insitu current and vice versa.

The coefficient of friction (COF) is defined as a ratio of the tangential friction force, resisting relative motion of the surfaces, to the normal load pressing the surfaces together. To monitor friction, it is preferred to measure its coefficient instead of just measuring the force resisting the relative motion of rubbing surfaces. Indeed, there are cases when changes in down-force cause substantial changes in the friction force, while the coefficient of friction remains constant. Alternatively, sometime important changes in the coefficient of friction cannot be observed by monitoring the friction force due to periodic fluctuations of the down-force.

The total wear of the interface, typically measured in the direction perpendicular to the rubbing surfaces, consists of wafer and pad linear wear. To monitor wear, it is preferred to measure the linear geometrical wear of each of the rubbing surfaces. As wafer material removal is of the order of nanometers, its measurements are very complicated during polishing, and are often performed after polishing. The pad wear is of the order of micrometers, and its measurements are straightforward.

Another important parameter of friction and wear is the acoustic emission (AE) from the contact of rubbing surfaces [3][4]. Its spectrum may have numerous frequencies, corresponding to such different processes as plastic and elastic deformations of sub-surface material layers, micro-scratching and micro-fatigue, micro-corrosion and other electrochemical reactions, delamination of material layer. The mega-Hertz acoustics is more informative of the specific micro-tribo-processes on tiny micro-contacts, in comparison with a kilo-Hertz range reflective of integral characteristics of the interface and deci-Hertz range reflective of integral characteristics of the entire mechanical system. Among the main benefits of the acoustic measurements in CMP are monitoring the intensity of polishing processes and detecting polishing conditions when wafer layers, for example low-K polymers, delaminate.

Computerized real-time measurements and analysis of the coefficient of friction, contact high frequency acoustic emission and pad wear allow for the effective evaluation of dynamic characteristics of the polishing process. This Multi sensing technology can be used to develop new ECMP pads, slurry, conditioner, processes etc.

Results and Discussion

Figure 2 shows for real-time, in-situ monitoring of the wafer surface without optical observation. The transition in frictional values shows the material removal. Moreover, as the transition from an upper layer to a lower layer does not happen instantaneously and takes some time, this time is a direct characteristics of the non-uniformity of material removal. Parallel AE measurements compliment the friction ones (see Fig. 2) in detecting the defectivity rate and end point of polishing.

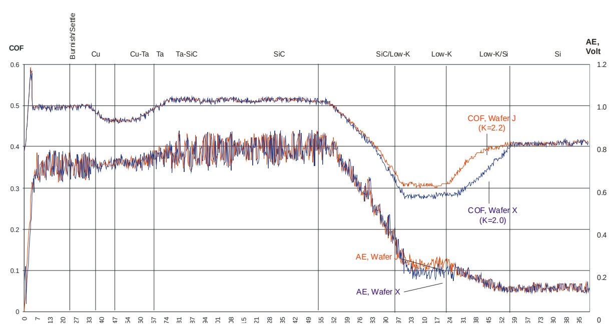

Figure 2 COF and AE plot on low K wafer CMP

Figure 3a shows the use of multi sensing technology on copper eCMP at constant current process. As copper thins down towards the end of process the voltage increases. Figure 3b shows the copper removal rate vs current density. These polishing experiments were done at sub 1psi pressure.

Just like CMP , ECMP process will depend heavily on the pad design. The opening on the pad dictate the anode to cathode ratio.

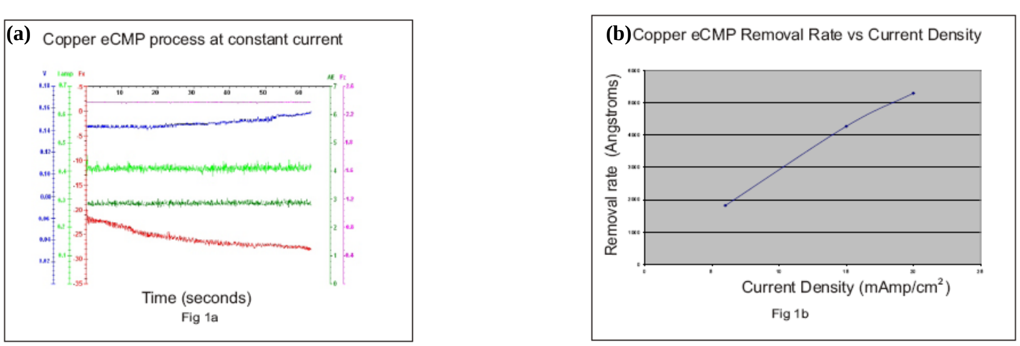

Figure 3 (a) Graph showing Copper eCMP (b) Copper removal rate vs current Density

The groove patterns and the cell structure will dictate the level of electrolyte on top of the pad. The change in groove patterns or the pad material will change the material properties (hardness, young's modulus etc.). Figure 4 shows the comparison between pad compressions of different pads using a disk. This slopes can then be use to calculate elastic modulus of the pads.

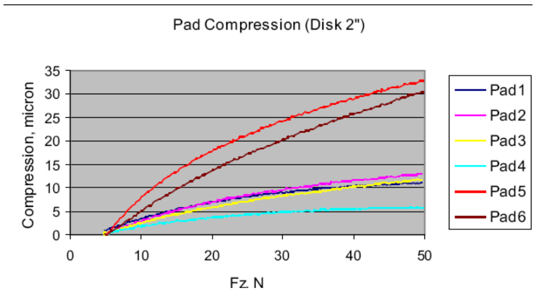

Figure 4 Comparing Pad Compression of Different Pads

CMP or ECMP yield will depend on the efficiency of the conditioners. The newer pad conditioners needs to be less aggressive on the pads (eCMP pads are typically softer in nature). The conditioner has to be more inert in nature to withstand eCMP electrolytes. Figure 5a shows the insitu pad wear rate after 2 hour of conditioning. Figure 5b shows the conditioning efficiency which dictates the time required to condition the pad to bring it to its original values.

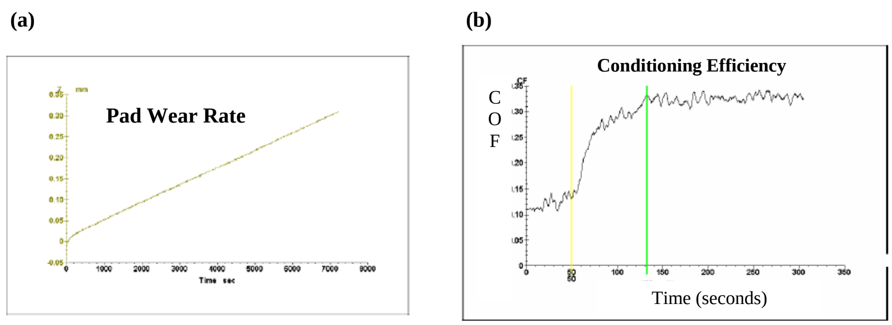

Figure 5 (a) Insitu Pad Wear Rate during conditioning (b) Pad conditioning Efficiency

Conclusion

The CETR eCP4 is a tool which can help the researchers to take eCMP to next level. The tool is capable to polish in sub 1psi range and can be used to develop pads, conditioners, slurries. The Multi sensing technology approach is a novel method to characterize the process completely. The bench top polisher is a cheaper viable option to do quick feasibility studies.

References

[1]S.V. Babu, K.C. Cadien, H. Yano, Eds. Chemical-Mechanical Polishing 2001: Advances and Future Challenges, Materials Research Society, Warrendale (2001).

[2] http://people.clarkson.edu/~samoy/ECMP.htm

[3] J. Fang, K. Davis, N. Gitis and M. Vinogradov, in Proceed. VLSI Multilevel Interconnection 20th Annual Conference, Marina Del Rey, September 2003.

[4] N. Gitis and M. Vinogradov, in Proceed. VLSI Multilevel Interconnection 20th Annual Conference, Marina del Rey, September 2003.